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☐	L36	(compiler near3 determin$4 near3 (appropriate or proper) near2 clock)	0
☐	L35	l33 same (instruction or command or task)	8
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END OF SEARCH HISTORY

L38: Entry 1 of 2 File: USPT May 1, 2001

DOCUMENT-IDENTIFIER: US 6226738 B1
TITLE: Split embedded DRAM processor

Detailed Description Text (21):
where the location $1000 corresponds to a cache memory interface location located on the embedded DRAM 310. Several type III instructions may be executed to generate the operand. Preferably, the bus 325 can be used to control the transfer of the operand directly to CPU core 300 without the need for intermediate handshaking. That is, the CPU core 300 does not send out the address $1000, but reads the CPU bus 325 on an appropriate clock edge determined at compile time. Also, the compiler may issue a command early to allow the embedded-DRAM coprocessor 310 time to prepare an operand in advance so that the operand will be ready when it is needed in the instruction processing on the CPU core 300. That is, using the concepts of SDRAM technology, the data will become available a fixed delay later and will be synchronized with a clock edge. This allows the processor core 300 to continue with other instructions, for example using superscalar dispatching and out-of-order execution. The type II instruction will remain in the active buffer until its dependence information comes in, synchronized with the internal processor pipelines after a fixed delay.

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L24: Entry 1 of 8 File: USPT Nov 25, 2003

DOCUMENT-IDENTIFIER: US 6653871 B2
TITLE: Method of and circuit for controlling a clock

Current US Original Classification (1):
327/99

Current US Cross Reference Classification (1):
327/291

CLAIMS:

10. A clock control circuit, comprising: a low speed clock supply unit which outputs a low speed clock; a high speed clock supply unit which outputs a high speed clock whose frequency is higher than the low speed clock; a selection unit which selects and outputs one of the low speed clock output from the low speed clock supply unit and the high speed clock output from the high speed clock supply unit; a control unit which controls the selection of the clock by the selection unit; a dividing unit which divides the high speed clock, selected and output from the selection unit in accordance with a dividing ratio; a dividing ratio set unit which sets the dividing ratio of the dividing unit so that a clock, which is supplied by the dividing unit to a circuit whose clock is to be switched from the low speed clock to the high speed clock, becomes faster gradationally; and a sleep control unit which allows the circuit to go into a sleep state every time the dividing unit outputs a clock with a different dividing ratio to the circuit, just after the clock with the different dividing ratio is output, and thereafter allows the circuit to go into a normal state.

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L24: Entry 2 of 8 File: USPT Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6515530 B1
TITLE: Dynamically scalable low voltage clock generation system

Brief Summary Text (8):
A phase locked loop (PLL) has a programmable frequency divider (PRFD) that divides the output of the PLL to generate a feedback clock (FBCLK) which is compared to a reference clock (RCLK) in a phase/frequency comparator. The PLL output is divided in a second PRFD to generate a divided PLL output clock. The PLL is powered from a scalable logic power supply voltage of a system that employs dynamic frequency and voltage scaling to manage energy consumption of the system. The PLL power supply and reference voltages are generated by voltage regulating the scalable logic power supply voltage. The PLL supply voltage is less than the lowest voltage level of the scalable logic power supply voltage used in the system. The PLL is designed to operate at the highest frequency of the system when the system uses the highest level of the scalable logic power supply voltage. A fixed frequency clock and the PLL output clock are multiplexed (MUX) in a glitch-less circuit under system control to supply the system clock. The scalable logic power supply voltage may be varied without affecting operation of the PLL. If the scalable logic power supply voltage level is to be lowered below a level that supports the existing system clock frequency, then the system clock frequency is first lowered by programming the frequency divider that divides the PLL output. The divisor of the second PRFD may be dynamically changed without switching to the fixed frequency clock. A valid signal from the second PRFD is generated indicating when its divisor may be changed without causing glitches in its output. If the frequency of the PLL is to be altered, then the MUX selects the fixed frequency clock as the system clock, then programs the PLL and waits for it to stabilize, then the PLL output clock is again switched back as the system clock. The system clock signal is stopped, if necessary, in a known logic state by an appropriate signal sent to circuits in the MUX selecting the system clock signal. The logic employed in stopping and starting the system clock signal use a clock separate from the system clock signal. The scalable logic power supply voltage and the system clock frequency are dynamically scaled to manage system energy consumption and to optimize performance at a given energy consumption level. In one embodiment the scalable logic power supply voltage may be supplied by a battery whose voltage may change due to battery discharge. The battery voltage is monitored and the system clock frequency is dynamically scaled when necessary without affecting the PLL.

Current US Original Classification (1):
327/291

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L24: Entry 3 of 8 File: USPT Aug 17, 1999

DOCUMENT-IDENTIFIER: US 5940607 A
TITLE: Device and method for automatically selecting a central processing unit driving frequency

Detailed Description Text (5):
In the operation of the device for selecting and supplying an appropriate frequency to the central processing unit, the user sets the third and the fourth switch of the frequency selecting unit 1 in order to supply a selection signal to the clock generator 7 of the clock supply unit 3, and then the user sets the first and the second switch of the frequency selecting unit 1 in order to supply a selection signal to the central processing unit 5. The clock generator 7 of the clock supply unit 3 receives the selection signal and transmits a clock signal to the clock buffer 9 of the clock supply unit 3. The clock buffer 9 of the clock supply unit 3 receives the clock signal and transmits an external supply frequency to the central processing unit 5. At this time, the central processing unit 5 receives the external supply frequency from the clock buffer 9 and the selection signal from the first and second switch, and operates after determining the internal operation frequency.

Current US Original Classification (1):
713/501

L24: Entry 3 of 8 File: USPT Aug 17, 1999

DOCUMENT-IDENTIFIER: US 5940607 A
TITLE: Device and method for automatically selecting a central processing unit driving frequency

Detailed Description Text (5):
In the operation of the device for selecting and supplying an appropriate frequency to the central processing unit, the user sets the third and the fourth switch of the frequency selecting unit 1 in order to supply a selection signal to the clock generator 7 of the clock supply unit 3, and then the user sets the first and the second switch of the frequency selecting unit 1 in order to supply a selection signal to the central processing unit 5. The clock generator 7 of the clock supply unit 3 receives the selection signal and transmits a clock signal to the clock buffer 9 of the clock supply unit 3. The clock buffer 9 of the clock supply unit 3 receives the clock signal and transmits an external supply frequency to the central processing unit 5. At this time, the central processing unit 5 receives the external supply frequency from the clock buffer 9 and the selection signal from the first and second switch, and operates after determining the internal operation frequency.

Current US Original Classification (1):
713/501

L24: Entry 6 of 8 File: USPT Jun 30, 1998

DOCUMENT-IDENTIFIER: US 5774701 A
TITLE: Microprocessor operating at high and low clok frequencies

Detailed Description Text (12):
The multiplexer MUX3 selects the clock pulse ck1 outputted from the divider DIV1 when the clock enable signal CKEN is high and the select control signal COSEL1 is low and supplies the selected clock pulse ck1 as a system clock signal CK1 (a first system clock signal) to a first internal circuit including the central processing unit CPU. When the clock enable signal CKEN is high and the select control signal COSEL1 is high, the multiplexer MUX3 selects the clock pulse DV1 outputted from the PLL circuit to supply the selected clock pulse to the central processing unit CPU as the system clock signal CK1. It should be noted that, when the clock enable signal CKEN is low, the output of the multiplexer MUX3 is fixed to the low level. As a result, at switching from the low-speed operating mode to the high-speed operating mode, the system clock signal CK1 is temporarily halted, thereby stabilizing the operation of the CPU and other components at the time of mode switching.

Current US Original Classification (1):
713/501

Current US Cross Reference Classification (1):
713/601

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L7: Entry 4 of 6 File: USPT Oct 5, 1999

DOCUMENT-IDENTIFIER: US 5963075 A
TITLE: Large scale integrated circuit having functional blocks controlled with clock signals that conduct setting operations at different times

Brief Summary Text (16):
In the conventional example described above, the average or mean power consumption of the overall LSI chip can be controlled by distributing clock signals having mutually different frequencies to the respective functional blocks. However, considerations have not been particularly given to the fluctuation of the power source potential in the transient state and to the transient current, which consequently leads to drawbacks as follows. Although the average power consumption is reduced, there occurs a wrong operation due to variation in the power source potential or the circuit size is limited due to influence of the radiation noise from the power source line in association with the transient current. The operating voltage of power source has tended to decrease because of the finer machining technology of circuits thanks to the recent development of process technologies and requirements in the market. In consequence, when it is assumed that the variation in the power source potential is kept unchanged, the ratio of the variation to the operating power source potential becomes larger. This resultantly causes the wrong operation and hence restricts the circuit size.

Brief Summary Text (22):
The LSIC of the present invention includes independent clock supply means for supplying a plurality of kinds of clock signals corresponding to respective functions of the functional blocks. The clock supply means includes a clock distributor circuit distributing a plurality of output clock signals in which at least one output clock signal selected from the plural clock signals produced therefrom has a phase different from those of the remaining clock signals, and it is inhibited that all clock signals conduct the setting operation at the same time. As a result, the maximum transient current appearing in relation to the simultaneous setting operation of the clock signals is reduced.

Brief Summary Text (23):
Moreover, the clock supply means includes a clock distributor circuit distributing a plurality of output clock signals in which at least one output clock signal selected from the plural clock signals produced therefrom has a clock cycle or period different from those of the remaining clock signals and at least one output clock signal selected from the plural clock signals produced therefrom has a phase different from those of the remaining clock signals, and it is inhibited that all clock signals conduct the setting operation at the same time. Resultantly, the power consumption related to the setting operation can be minimized.

Detailed Description Text (5):
FIG. 7 shows an operation timing chart of the clock supply means including a combination of the flip-flop circuit and the AND circuits. As can be seen from FIG. 7, the CLKM signal 111 and the CLKN 112 have mutually different phases of pulses and only two kinds of clock signals selected from the three kinds of clock signals CLKL 110, CLKM 111, and CLKN 112 are related to timing of simultaneous change. This makes it possible to suppress the transient current which influences the width of deviation in the power source potential as well as the increase in the radiation

noise from the power source line. Assuming that the CPU 103, the peripheral block A 104, and the peripheral block B 105 have the same load capacitance, the maximum transient current can be decreased to about 2/3 that appearing when the clock signals supplied to these blocks are changed at the same time. Conversely, assuming that there is allowed a voltage deviation width equivalent to the conventional case in which the clocks are simultaneously varied, the circuit size can be increased to about 1.5 that of the conventional circuit.

CLAIMS:

9. A method of lowering power consumption in a large scale integrated circuit (LSIC) comprising the steps of supplying a plurality of clock signals to functional blocks of the LSIC, at least one of which is a control block for conducting data accessing operation to and from another one of the functional blocks, wherein two of the plurality of clock signals have different frequencies and all of the plurality of clock signals never conduct a setting operation at the same time.

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L7: Entry 2 of 6 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243399 B1
**** See image for Certificate of Correction ****
TITLE: Ring signal generator

Detailed Description Text (56):
Various signal processing functions in the subscriber unit 10 require different signal frequencies for, e.g., clock frequencies, local oscillator frequencies, and reference frequencies, for both transmit and receive operations, as is well known in the art. The process of producing those frequencies advantageously involves direct digital synthesis (DDS) functions, also as known in the art. In the embodiment of FIG. 1, the DIF section 36 advantageously performs the DDS function for subscriber unit circuit components involved in only transmitting operations. In addition, a separate DDS section 44 performs the DDS function for subscriber unit circuit components that are involved in primarily only receive operations. Output of the DDS 44 is coupled via a DDS-fed DAC (SDAC) 45 to the receive portion 13 of RF section 11. Since at least one circuit component, to be described, of the receive portion has such long time constants that it must be powered up at all operating times, the DDS also is powered up during all operating times (vis-a-vis initializing).

Detailed Description Text (59):
Control logic circuits 32 supply clock signals to circuit components of the DDF ASIC 20. A circuit 35 couples continuous clock signals to the DDS 44. A circuit 46 couples selected, i.e., programmably interruptible, clock signals to the DIF section 36, and a circuit 47 couples other selected clock signals to both the INT section 34 and the FIR section 33, as will be described in connection with FIG. 8. By turning clock signals on circuits 46 and 47 on and off in appropriate time slots the FIR and INT sections and the DIF section, all of which are advantageously implemented in the CMOS technology, are effectively powered up and down for power consumption control. When CMOS circuitry is not clocked, the CMOS transistors do not switch, and the circuit assures a nearly zero power consumption level.

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L7: Entry 3 of 6 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6026498 A
**** See image for Certificate of Correction ****
TITLE: Clock signal generator circuit using a logical result of an output of a computer and a source clock to generate plurality of clock signals

Brief Summary Text (15):
According to the present invention, there is provided a clock signal generator circuit for generating and supplying clock signals to a central processing unit and functional blocks, comprising a clock generator for suppressing at least one active or inactive state of a source clock signal, to generate and provide a plurality of clock signals whose periods are integer multiples of a period of the source clock signal; and clock selectors each selecting one clock signal of the clock signals generated by the clock generator and supplying to at least one of the central processing unit and the functional blocks.

Detailed Description Text (15):
This problem may be solved by supplying clock signals having different periods to the CPU and functional blocks. However, the synchronous bus will cause a malfunction if the CPU and functional blocks are operated at different speeds.

CLAIMS:

1. A clock signal generator circuit for generating and supplying clock signals to a central processing unit and functional blocks, comprising:

a clock generator for suppressing at least one active or inactive state of a source clock signal by calculating a logical result of an output of a counter and the source clock, to generate and provide a plurality of clock signals whose periods are integer multiples of a period of the source clock signal; and

a plurality of clock selectors, provided for said central processing unit and said functional blocks, each selecting one clock signal of the clock signals generated by said clock generator and supplying to at least one of said central processing unit and said functional blocks.

3. A microcontroller system comprising a central processing unit, functional blocks, and a clock generator for generating and supplying clock signals to said central processing unit and said functional blocks, wherein said clock generator suppresses at least one active or inactive state of a source clock signal by calculating a logical result of an output of a counter and the source clock, to optionally generate a plurality of clock signals whose periods are integer multiples of a period of the source clock signal, and supplying the generated clock signals to said central processing unit and said functional blocks through a plurality of clock selectors, and each of said clock selectors selects one clock signal of the clock signals generated by said clock generator.

8. A semiconductor integrated circuit device having a central processing unit, functional blocks, and a clock generator for generating and supplying clock signals to said central processing unit and said functional blocks, wherein said clock generator suppresses at least one active or inactive state of a source clock signal

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L8: Entry 2 of 4 File: USPT Mar 26, 2002

DOCUMENT-IDENTIFIER: US 6361440 B1
TITLE: Game system, game machine, game data distribution machine, network system and information storage medium

Detailed Description Text (21):
The game machine 200 also comprises a clock generation section 220 for generating the operation clock which determines the operating speed of the game data production section 290 and others per each game executing means such as the game data production section 290 and a clock selection section 260 for selecting clock to be applied from a plurality of clocks whose speed is different based on the received indication data and for supplying the selected clock to the clock generation section 220. The clock selection section 260 functions as clock adjusting means for adjusting the clock speed.

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L8: Entry 3 of 4 File: USPT Nov 4, 1997

DOCUMENT-IDENTIFIER: US 5684418 A
TITLE: Clock signal generator

Detailed Description Text (77):
As explained above, according to the present embodiment, n number of multipliers 11-1 to 11-n have variable multiple factors and multiplying a single input external reference clock signal by means of the multiplying factors (xi) to (xn). The m number of frequency dividers have variable dividing factors for dividing a clock signal, which is generated by the multiplier 11-2 multiplying by the multiplying factor (x 2) and synchronized with the external clock signal CK, by means of the dividing factors (x 1/1) to (x 1/m). A clock generator 1 is comprised of a synchronous circuit 13 making k (n+m) number of clock signals, which are generated by the multipliers 11-1 to 11-n and the frequency dividers 12-1 to 12-n having different frequencies, synchronized with the reference clock signal CK. A clock selector 2 receives a plurality of clock signals generated by the clock generator 1 and status signals STS sent from each of the functional blocks of a system, not shown, and applies different signals by switching the frequency according to the operational status of each of functional blocks selectively The clock selector 2 also generates an operation control signal for making the multipliers 11-1 to 11-n and the frequency dividers 12-1 to 12-m in the clock generator 1, which generate unused frequencies, stop and outputs the signal OF to the clock generator 1. It is therefore possible to supply a plurality of clock signals having required frequencies and prevent needless power consumption of each clock by switching the frequency supplied to the block according to the status of operation of each block in the system.

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L8: Entry 1 of 4 File: USPT Jul 29, 2003

DOCUMENT-IDENTIFIER: US 6600575 B1
TITLE: Clock supply circuit

CLAIMS:

1. A clock supply circuit for feeding a clock signal to a functional block of an electronic apparatus having a functional block being operating based on a clock signal produced by dividing a system clock comprising: a clock dividing section for generating said clock signal to be fed to said functional block by dividing said system clock; and a control section for controlling a supply of said clock signal from said clock dividing section to said functional block depending on an active state of said functional block where a desired operation is required or on an idle state where no operation is required wherein said clock dividing section is adapted to generate a plurality of clock signals each having a different frequency and wherein said control section comprises selectors adapted to selectively output said plural clock signals fed by said clock dividing section, and a decision section adapted to control a selection operation of said selectors so that, in an active state of said functional block where said desired operation is required, a clock signal selected out of said plural clock signals having proper frequency is supplied to ensure adequate operations of said functional block and so that, in an idle state, a clock signal having a frequency being lower than that of said clock supplied in said state where said desired operation is required is fed to said functional block and wherein said electronic apparatus is equipped with a plurality of functional blocks and wherein said clock dividing section is adapted to generate a plurality of clock signals each having a different frequency and wherein each functional block is provided with one of the selectors for providing the selected frequency to the functional block.

13. A clock supply circuit for supplying clock signals to an electronic apparatus having a plurality of functional blocks, each functional block operating based on said clock signal, comprising: a clock dividing section to receive and divide a system clock, and to output a plurality of clock signals with different frequencies; a decision section for selecting one appropriate frequency from the plurality of clock signals to be supplied to one of the plurality of functional blocks based on an operating state signal of the one of said plurality of functional blocks and for outputting a decision signal as a frequency selection signal; and at least one selector receiving at least two clock signals outputted from said dividing section and receiving said decision signal outputted from said decision section, selecting one of the received clock signals based on the received decision signal, and outputting said selected clock signal to said electronic apparatus for supplying said selected clock signal to said one of said functional blocks.

14. The clock supply circuit according to claim 13, wherein said clock dividing section is adapted to generate a plurality of clock signals each having a different frequency and wherein said control section comprises selectors adapted to selectively output said plural clock signals fed by said clock dividing section, and a decision section adapted to control a selection operation of said selectors so that, in an active state of said functional block where said desired operation is required, a clock signal selected out of said plural clock signals having proper

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L32: Entry 3 of 3 File: USPT Jan 2, 1996

DOCUMENT-IDENTIFIER: US 5481697 A

TITLE: An apparatus for providing a clock signal for a microprocessor at a selectable one of a plurality of frequencies and for dynamically switching between any of said plurality of frequencies

Brief Summary Text (8):

One of the objectives of the present invention is to provide a variable frequency clock generator that may be dynamically switched between frequencies such that the duration of every clock cycle is at least as great as the clock cycle duration of the highest operating frequency.

Current US Original Classification (1):

713/501

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L21: Entry 2 of 5 File: USPT Feb 27, 2001

DOCUMENT-IDENTIFIER: US 6195753 B1
TITLE: Information processing apparatus with reduced power consumption

Brief Summary Text (18):
According to the second aspect of the present invention, there is provided an information processing apparatus comprising an instruction memory for storing an instruction, an instruction register in which the instruction in the instruction memory is loaded, a plurality of function blocks for performing a basic operation required for execution of the instruction, an instruction/state decoder for decoding the instruction read out from the instruction register, and also decoding a control signal for notification of a state between the function blocks, a plurality of clock generators for generating first and second clocks having different frequencies, and a clock supply/stop circuit for supplying the first clock having a high frequency to only a function block, of the plurality of function blocks, which is required for execution of the decoded instruction and needs to operate, and supplying the second clock having a low frequency to a function block which need not operate, on the basis of an output signal from the instruction/state decoder.

Current US Original Classification (1):
713/322

CLAIMS:

1. An information processing apparatus comprising:

an instruction memory which stores at least one instruction;

an instruction register which receives one of said instructions from said instruction memory;

a plurality of function blocks, at least a one of said function blocks being a select function block able to perform an operation required for execution of said instruction, each function block producing a respective control signal indicative of whether another select function block should be enabled;

an instruction/state decoder which receives said instruction from said instruction register, receives said control signals and outputs an output control signal in, response thereto; and

a clock supply circuit which receives said output control signal and, in responses to said output control signal, selectively couples a first clock to said select function block to perform the operation required for execution of said instruction.

2. An information processing apparatus comprising:

an instruction memory which stores at least one instruction;

an instruction register which receives at least one of said instructions from said

instruction memory;

a plurality of function blocks, at least one of said function blocks being a select function block able to perform an operation required for execution of said instruction, each function block producing a respective control signal indicative of whether another select function block should be enabled;

an instruction/state decoder which receives said instruction from said instruction register, receives said control signals, and outputs an output control signal in response thereto;

a plurality of clock generators which generate first and second clocks, respectively, said first clock having a higher frequency than said second clock; and

a clock supply circuit which receives said output control signal and, in response to said output control signal, selectively couples said first clock to said select function block and couples said second clock to all of said function blocks except for said select function block to perform the operation required for execution of said instruction.